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Leveraging Standards-Based MOSA for SWaP-Constrained Deployable Systems with VNX+

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ABSTRACT

OpenVPX (VITA 65), especially in Sensor Open System Architecture, or SOSA®, aligned variants, is a popular choice for advanced vehicle-based sensor processing and communications systems. SOSA based OpenVPX has proven itself repeatedly over the years to be a reliable, rugged modular open-systems architecture for these sorts of mounted applications. However, there are many examples when space, weight, and power (SWaP) constraints limit the ability to leverage OpenVPX. This is especially true for autonomous vehicles, which by their nature are smaller than crewed vehicles. To address this need SOSA has incorporated VITA 90 (VNX+) into the Technical Standard. Released as an ANSI-approved standard in early 2026, VNX+ brings to the SOSA standard the same connectivity and system infrastructure elements as OpenVPX, but in a package roughly 1/3 the size. By using VNX+, system integrators gain all of the benefits of MOSA as defined by SOSA principles in a form factor suitable for these challenging SWaP-constrained problems.

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1. INTRODUCTION

In late 2019 the Sensor Open System Architecture Consortium (https://www.opengroup.org/sosa) decided to form the Small Form Factor Subcommittee. This working group was chartered to explore options for hardware "physically smaller than 3U VPX" and to draft requirements language for inclusion into the technical standard. The subcommittee wanted to be sure that the language in the technical standard was relevant to the applications targeted by the SOSA Technical Standard [1], so during the early work of the subcommittee numerous applications and use cases were explored. Crewed and uncrewed ground vehicles were included among these use cases.

In this paper, we will examine the details of VNX+ along with the specific VNX+ elements defined within the SOSA Technical Standard. In addition, we will look at how ground vehicle-based systems can make use of these elements to solve critical sensor processing, communications, and mission computing problems.

2. VNX+ OVERVIEW

The VNX+ standard is captured by a set of documents published by the VITA Standards Organization (VSO):

- ANSI/VITA 90.0-2026: VNX+ Base Standard [2]
- ANSI/VITA 90.1-2026: VNX+ Profile Tables [3]
- VITA 90.2-2026 VDSTU: VNX+ Optical and Coax Apertures [4]
- ANSI/VITA 90.3-2026: VNX+ Power Supply and Storage Modules [5]
- ANSI/VITA 90.4-2026: VNX+ Cooling and Mounting Systems [6]
- ANSI/VITA 90.7-2026: VNX+ Optical and NanoRF Coax Apertures Standard [7]

All are released and approved by ANSI, except for VITA 90.2 which is currently released by the VSO for trial use (VDSTU – VSO Draft Standard for Trial Use). Figure 1 shows several key features of the VNX+ form factor.

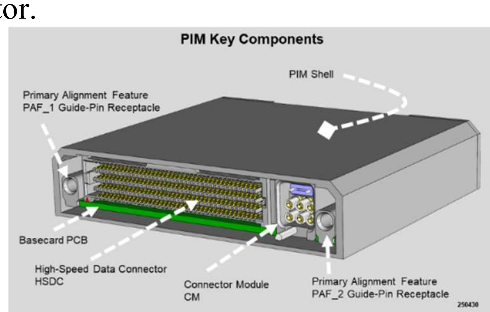


Figure 2: Basic VITA 90 module - key components. From ANSI/VITA 90.0-2026

VNX+ defines two basic plug in module (PIM) sizes: 13mm and 19mm high. It also defines double-height modules of 27mm and 39mm of two types, Style-A with the connector and guide features on the bottom half, and Style-B with the connector and guide features on the top half. 13mm (and 27mm double-height) modules offer a 200-pin connector, while the 19mm (and 39mm double-height) modules offer a 400-pin connector, a 320-pin connector with space for a half-size coax/optical connector module, and a 200-pin connector with a full-sized connector module. Figure 1 shows several of these variants.

VITA 90.3 defines a set of power supply,

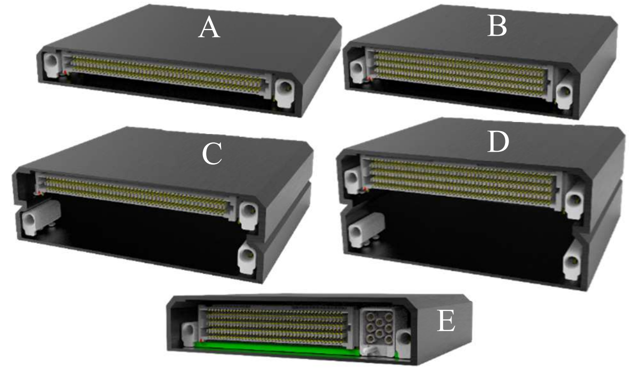


Figure 1: Examples of the VNX+ module types. (A) 13mm, (B) 19mm 400-pin, (C) 13mm double-height Style-B, (D) 19mm 400-pin double-height Style B, (E) 19mm 320-pin with a Style-2D Coax Connector Module.

power conversion, and power filtering PIMs of various types and specifications. However, in this document we will limit our focus to the non-power modules.

Since SOSA narrows the module selection to only the 19mm single-height and 39mm Style-B double-height form factors, we will focus on those when we explore the details below in keeping to the topic of MOSA for uncrewed vehicles. Note, however, that much of the detail below also applies to 13mm and 27mm modules and slot profiles.

VITA 90.0 defines the basic PIM form factor defined above. VITA 90.0 PIMs are mounted into a chassis with the three walls of the chassis pressing against the PIMs to form both a retention mechanism as well as a thermal path for cooling the PIMs. Thermal interface material is typically used to absorb any mechanical tolerance between the chassis walls and the PIMs with only modest reductions in thermal efficiency.

VITA 90.4 defines an alternative module form factor that adds mounting flanges to the base VITA 90.0 external shape. These flanges can be used to mount a wedgelock, or even for mounting to a flat surface such as a bulkhead. The addition of wedgelocks to the base VITA 90 design greatly eases the task of inserting, securing, and removing a VNX+ plug-in module from a chassis. However, the minimal metal-on-metal contact area between the flange and the chassis rail presents significant thermal resistance when compared to the large three-sided contact area found with the basic VITA 90 design.

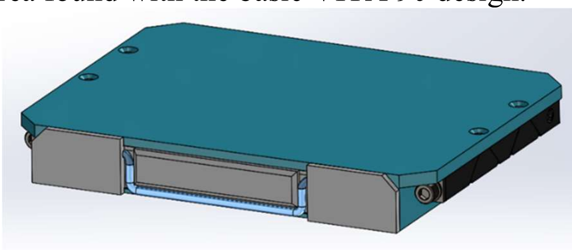


Figure 3: Wedgelock version of a VITA 90 module.

VITA 90.0 also defines the common pin assignments and payload card regions of the connector. All VNX+ modules have a region known as the S1 Utility Segment, which is where utility functionality such as power, resets, chassis management bus (IPMB), and other signals such as NVMRO (non-volatile memory read only) reside. Most profiles have these pins in the same location on the connector, although some have this region slightly rearranged. It should be noted that the S1 Utility Segment includes all of the same utility functionality found in OpenVPX (and then some), ensuring a commonality in architecture elements between the two form factors. This is important for MOSA-based system design.

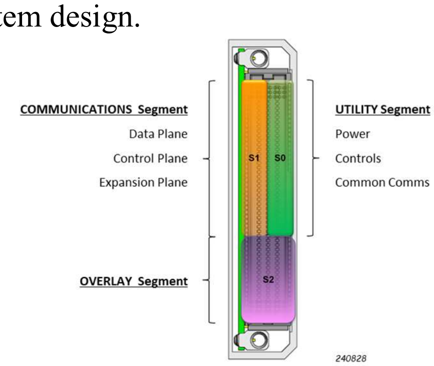


Figure 4: Rough mapping of the segments to a 19mm VITA 90 connector. Note that the 13mm connector has a similar template. From ANSI/VITA 90.0-2026

VITA 90.1, in turn, defines a set of slot profiles and approved protocols for VNX+. Many of these profiles (mainly payload modules - as opposed to the more specialized profiles such as switch and radial clocks) are defined based on a common template defining not only the S1 Utility Segment mentioned above, but also an S2 Communications Segment and an S3 Overlay Segment. The S2 Communications Segment is where the Data Plane (DP), Control Plane (CP), and Expansion Plane (EP) ports reside, which form the primary inter-module communications pathways in VNX+ systems.

The S3 Overlay Segment is a region composed of copper pins (in 400-pin profiles), an aperture for coax and/or optical (in 240-pin profiles), or a split copper/aperture region (in 320-pin profiles). The S3 Overlay Segment is where slot profiles differentiate by providing different arrays of communications ports or capabilities.

It should be noted that the VNX+ architecture closely matches the latest editions and profiles of VITA 65/OpenVPX. This was a deliberate choice by the standard committees to promote and leverage the MOSA principles found in SOSA. This commonality includes critical S0 Utility Segment signals such as NVMRO and GDiscrete1, as well as the DP/CP/EP structure for inter-module communications. Like OpenVPX, these planes have general (although not mandated) functionality in high-performance embedded systems:

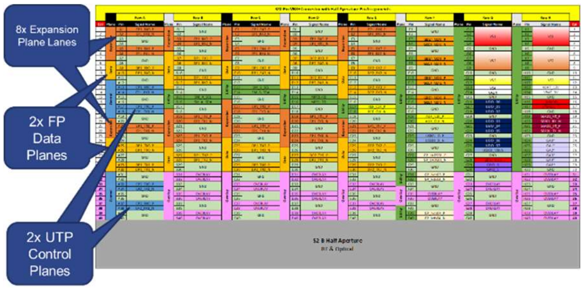


Figure 5: 320 pin profile S2 Communications Segment based on the profile template.

- Data Plane: Fat Pipes (FP – four bidirectional lanes) for high-speed streaming data. This is where the primary application data is exchanged between PIMs, and sometimes where incoming data passes as it is sent to PIMs for processing.
- Control Plane: Ultra-Thin Pipes (UTP – single bidirectional lanes) for exchanging command and control messages. The CP is separate from the DP so to not interfere with the high-speed streaming data.
- Expansion Plane: A series of lanes that can be flexibly utilized for more closely-coupled links between PIMs. Typical uses include PCI Express between PIMs (GPU expansion, I/O, etc.) or dense FPGA-to-FPGA links. EP can also be used for direct LVDS links providing extremely low-latency channels (critical for many applications including EW and Radar).

3. VNX+ AND SOSA

The SOSA Technical Standard is a standard (and a reference architecture) intended to promote MOSA in building components and systems for high-performance sensor platforms such as EO/IR, Electronic Warfare, Radar, SIGINT (and other 'INTs), Communications, and Directed Energy. SOSA is designed around a set of fundamental principles to achieve its MOSA goals:

- Modular
- Interoperable
- Replaceable
- Securable
- Portable
- Plug-and-Play
- Scalable
- Resilient
- Vendor Agnostic
- Royalty Free
- Protection of IP
- Extensible and Evolvable
- Simple through complex systems
- Small through large systems

VNX+ has many options, such as different slot profiles, I/O protocols, power settings, etc. To promote the various MOSA attributes such as interoperability and replaceability, SOSA has reduced these options to a minimum set. In the following sections we will review this minimum set and describe the reasoning for SOSA's choices.

3.1. SLOT PROFILES

Arguably the most important rules in the SOSA Technical Standard involving VNX+ are the permitted 19mm and 39mm slot profiles. There are six slot profiles defined within SOSA (excluding space-specific profiles):

- 400 Pin Payload: VNX.PL-1-HH.400-7.2.1.1-<General Payload>
  - Includes pins designated for mezzanine-mapped I/O
- 320 Pin Payload: VNX.PL-1-HH.320-8.2.2.1-<General Payload>
  - Half-size aperture for coax and optical
- 400 Pin Switch: VNX.SW-1-HH.400-7.4.1.1-<7DP/8CP Switch>
  - 7x Data Plane, 8x Control Plane
- 320 Pin Switch: VNX.SW-1-HH.320-7.4.2.1-<5DP/5CP Switch>
  - 5x Data Plane, 5x Control Plane
  - Dual MT Optical

- 7-Slot 320-pin Radial Clock: VNX.RC-1-HH.320-7.5.2.2-<7REFCLK/7AUXCLK Overlay>
    - Based on the Payload Template
    - 7x REFCLK/AUXCLK pairs
    - Half-size aperture for coax
- High-density 320 pin Radial Clock: VNX.RC-1-HH.320-7.5.2.1-<22REFCLK/22AUXCLK>
    - Not based on the template
    - 22x REFCLK/AUXCLK pairs
    - Half-size aperture for coax

While this at first glance may seem like a lot of options, each was in fact carefully chosen to address specific needs within the SOSA application space:

- 400 Pin Profile: General SBC-type of payload, with an assortment of I/O and pins for QMC [8] I/O
- 320 Pin Profile: Similar to the 400 Pin Profile, but with a reduced set of I/O, no mezzanine mapped I/O for QMCs, but a half-size aperture for coax and/or optical connections
- 400 Pin Switch: Maximum switch matrix ports
- 320 Pin Switch: Reduced switch matrix ports, but a half-size aperture for optical connections
- 7-Slot Radial Clock: A highly accurate clock source is a common requirement for SOSA systems. This profile implements seven slots of REFCLK/AUXCLK pairs in the S2 Overlay Segment region, preserving the S1 Communications Segment, allowing a full payload card's worth of Data Plane, Control Plane, and Expansion Plane I/O.
- 22-Slot: Replaces most of the S1 Communications Segment with REFCLK/AUXCLK pairs to support systems with large node counts.

3.2. PROTOCOLS

SOSA limits the protocols permitted on the Data Plane, Control Plane, and Expansion Plane to the following:

Table 1: SOSA approved protocols for the S2 Communications Segment Planes

Data Plane	1000BASE-KX 10GBASE-KX4 10GBASE-KR 40GBASE-KR4 25GBASE-KR 100GBASE-KR4
Control Plane	1000BASE-KX 10GBASE-KR
Expansion Plane	PCIe Gen2/3/4 Serial FPDP 10/25 LVDS

The Peripheral Port is currently limited to SATA Gen 1/2/3, but that is likely to change as the market begins to find uses for this new port.

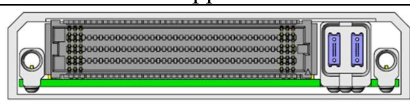
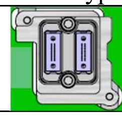
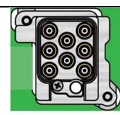
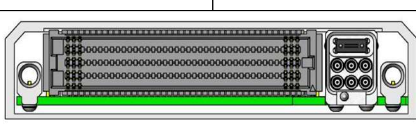
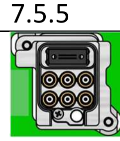
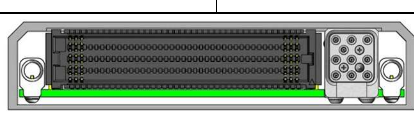
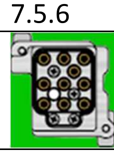
These ports and their functionality are all aligned with OpenVPX as defined in the SOSA Technical Standard. This commonality with OpenVPX ensures that VNX+ has a common design philosophy and architecture with that well established form factor.

3.3. CONNECTOR MODULES

Like OpenVPX and the Connector Modules defined in the various VITA 66 and 67 documents, VNX+ 19mm modules have provisions for coax and/or optical blind-mate Connector Modules. These modules, defined by VITA 90.2 and 90.7 provide an important feature enabling high-speed optical or direct analog connectivity to the world outside of the VNX+ chassis. Also, like OpenVPX, SOSA limits the Connector Modules approved by the standard to a minimum subset. At the moment the approved Connector Modules are all from the VITA

90.2 document, but future revisions may include select VITA 90.7 Connector Modules. The SOSA approved Connector Modules are shown in Table 2.

Table 2: SOSA Approved Connector Module Types

		
2-MT Ferrule	Type-2B	VITA 90.2 Section 7.5.3
		
1-MT, 6-50 Ohm	Type-2C	VITA 90.2 Section 7.5.4
		
8-75 Ohm	Type-2D	VITA 90.2 Section 7.5.5
		
1-MT, 6-75 Ohm	Type-2E	VITA 90.2 Section 7.5.6
		
10-50 Ohm	Type-2F	VITA 90.2 Section 7.5.7

3.4. SOSA VNX+ S0 Utility Segment Details

While the S1 Communications Segment and the S2 Overlay Segment tend to get most of the attention due to their central nature in any embedded system, the S0 Utility Segment has many elements that play a crucial role in embedded systems, particularly those targeting crewed and uncrewed ground vehicles. In this section we will review the S0 Utility Segment and point out some of these elements.

All VNX+ modules have an S0 Utility Segment. Most payloads (and some other types of modules) follow a particular template for the S0 Utility Segment, although all modules implement certain critical features. Figure 6 points out a number of these elements. Note that much of this segment mirrors what is found in OpenVPX. This, again, is by design to ensure a commonality with OpenVPX in architecture and design approach. There are some important differences that are worth pointing out.

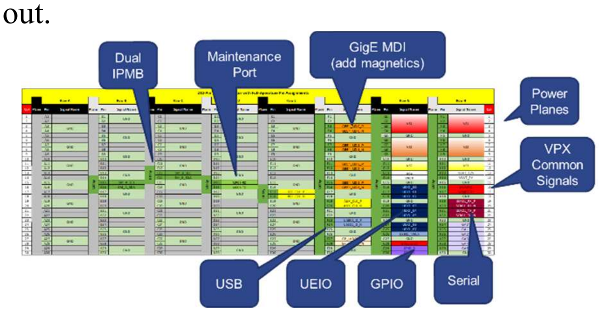


Figure 6: S0 Utility Segment based on the profile template.

First, let's point out the common elements:

Table 3: S0 Utility Segment signals and communications ports common with OpenVPX

Signals/Ports	Description
VS1, VS2, VS3, VS4, VAUX	Primary power delivery
VBAT_3V, VHeater	Power for real-time clock (VBAT_3V) and special heating circuits
GA*[4:0], GAP	Geographical address, parity

SM	System management bus – in SOSA this is dual VITA 46.11 IPMBs
GDiscrete1	Special low-latency discrete
SYSRESET	System Reset
NVMRO	Non-volatile memory read only (write protect)
REFCLK	Reference clock
AUXCLK	Auxiliary periodic clock
MP	Serial maintenance port (console, LVCMOS voltage levels)

Beyond these signals and ports common with OpenVPX, VNX+ implements a set of commonly-used communications ports. This was done to encourage a commonality in module design approaches and slot profiles not generally found in OpenVPX. These ports include:

Table 4: S0 Utility Segment signals and communications ports unique to VNX+

Signals/Ports	Description
GPIO, GPXLVDS	Single-ended and differential general-purpose I/O
USB1	USB 2
SER1	Dual RS-232, or single RS-422/485
GBE1	1000BASE-T – MDI, minus magnetics (added separately outside the module for space reasons)
UEIO	Unique external I/O (see below)

One very interesting port defined in Payload profiles S1 Utility Segment is known as the Unique External I/O (or UEIO) port. This port, not found in OpenVPX, consists of eight pins and can be defined in various ways implementing I2C and/or SPI interfaces which are useful in smaller VNX+ based systems for talking to port expanders, low-speed protocol ports (such as CANBus), small user displays, and similar devices often found in small systems.

There are six configurations defined in VITA 90.0:

1. 1x to 4x I2C
2. 1x to 2x SPI
3. 2x I2C and 1x SPI
4. 1x I2C and 1x SPI with 1x-2x SPI Selects
5. 1x SPI with 1x-5x SPI Selects
6. 2x SPI with 1x SPI Select each

However, to improve replaceability, SOSA reduces this to one:

- 1x I2C and 1x SPI with 1x-2x SPI Selects

In this way a payload module designer can implement I2C and/or SPI in a predictable way to enable easy reconfiguration or technology upgrades in the future.

4. VNX+ FOR CREWED AND UNCREWED GROUND VEHICLES

The small size of VNX+ when compared to even the already relatively small 3U OpenVPX form factor is the obvious advantage VNX+ enjoys when it comes to SWaP-constrained vehicle-mounted systems. However, there are a number of elements as defined by both VITA 90 and SOSA that make it an attractive architecture and a useful tool when applying MOSA to system design, including:

- Full-featured utility segment, with specialized signals critical to ground vehicle-based systems (GDiscrete1, NVMRO, etc.)
- UEIO, providing I2C and SPI interfaces for interfacing with specialized devices or busses (like CANBus)
- VITA 46.11 Tier-3 system management
- Built-in 1000BASE-T for connectivity to vehicle buses
- Familiar Data Plane / Control Plane / Expansion Plane architecture and protocols for high-performance interprocessor communications.

- Direct coax and optical connections via specialized connector modules (both 50 Ohm and 75 Ohm style)
- Mezzanine-mapped I/O for flexible addition of specialized I/Os
- Minimal but complete set of profiles and communications protocols, to promote MOSA in system integration and technology refresh

5. REFERENCES

[1] The Open Group SOSA® Consortium, Technical Standard for SOSA® Reference Architecture Edition 2.0 (Snapshot 3), 2025.

[2] VITA, ANSI/VITA 90.0-2026: VNX+ Base Standard, VME International Trade Organization, 2026.

[3] VITA, ANSI/VITA 90.1-2026: VNX+ Profile Tables, VME International Trade Organization, 2026.

[4] VITA, VITA 90.2-2026 VDSTU: Optical and Coax Apertures, VME International Trade Organization, 2026.

[5] VITA, ANSI/VITA 90.3-2026: VNX+ Power Supply and Storage Modules, VME International Trade Organization, 2026.

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[7] VITA, ANSI/VITA 90.7-2026: Optical and NanoRF Coax Apertures Standard, VME International Trade Organization, 2026.

[8] VITA, ANSI/VITA 93.0: QMC: Small Form Factor Mezzanine, 2025.

6. CONTACT INFORMATION

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7. ACRONYMS

AUXCLK	Auxiliary Clock. Generally 1 pulse per second
CP	Control Plane
DP	Data Plane
EO/IR	Electro-optic/Infrared
EP	Expansion Plane
EW	Electronic Warfare
FPGA	Field Programmable Gate Array
I2C (or I^2C)	Inter-integrated Circuit. A communications bus.
IP	Intellectual Property
IPMB	Intelligent Platform Management Bus
LVCMOS	Low-Voltage Complementary Metal-Oxide-Semiconductor
LVDS	Low-Voltage Differential Signaling
MT	Name for a style of optical interconnect
MOSA	Modular Open System Approach
NVMRO	Non-volatile Memory Read Only

PIM	Plug-in Module
REFCLK	Reference Clock. Varies by application.
SATA	Serial Advanced Technology Attachment. Storage interface.
SBC	Single-Board Computer
SIGINT	Signals Intelligence
SOSA	Sensor Open Systems Architecture
SPI	Serial Peripheral Interface. A communications bus.
SWaP	Space, Weight, and Power
UEIO	Unique External Input/Output
VDSTU	VITA Draft Standard for Trial Use
VITA	VME International Trade Association
VSO	VITA Standards Organization